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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/666,930	09/19/2003	Warren M. Farnworth	2269-5529US (02-0766.00/U	6453

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EXAMINER	
ISAAC, STANETTA D	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 05/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/666,930	FARNWORTH ET AL.	
	Examiner	Art Unit	
	Stanetta D. Isaac	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) *15-24,40 and 41* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 25-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/19/03 & 1/08/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the election filed on 3/7/05. Currently, claims 1-41 are pending.

Election/Restrictions

Applicant's election without traverse of 1-14 and 25-39 in the reply filed on 3/07/05 is acknowledged.

Claims 15-24, 40 and 41 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 3/07/05.

Information Disclosure Statement

The information disclosure statements (IDS) were submitted on 9/19/03 and 1/08/04. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Specification

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 12 recites the limitation "...the adhesive-coated tape extending over the ring of material" in lines 2-3. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-6, 10-14 and 29-34 are rejected under 35 U.S.C. 102(b) as being anticipated by Akram US Patent 6,140,151.

Akram discloses the semiconductor method as claimed. See figures 1-10 and corresponding text, where Akram teaches, pertaining to claim 1, a method for supporting wafers for singulation and pick-and-place, comprising: providing a semiconductor wafer **16** (figure 1; col. 2, line 60); mounting an adhesive-coated tape **12** to a surface of the semiconductor wafer (figure 1; col. 2, lines 48-50); singulating the semiconductor wafer into individual components **20**, leaving a ring of material about a periphery thereof (figures 1 and 2; col. 3, lines 1-33); and removing at least some individual components for the adhesive-coat tape (figure 8; col. 4, lines 50-67; col. 5, lines 1-4).

Pertaining to claim 2, Akram teaches, further gripping the semiconductor wafer by the ring of material during the removing of the at least some individual components (col. 4, lines 17-67; col. 5, lines 1-4).

Pertaining to claim 3, Akram teaches, further including forming the ring of material from material of the semiconductor wafer (figure 1; col. 2.lines 48-59).

Pertaining to claim 4, Akram teaches, further including forming at least a portion of the ring of material from a polymer material disposed about a periphery of the semiconductor wafer (col. 2, lines 50-55).

Pertaining to claim 5, Akram teaches, further including forming the ring of material in part from material of the semiconductor wafer and in part from a polymer disposed about a periphery of the semiconductor wafer (figure 1; col. 48-60).

Pertaining to claim 6, Akram teaches, further comprising forming the ring of material from the polymer material by one of spin-coating, sterolithography or molding (col. 2, lines 48-55, molding).

Pertaining to claim 10, Akram teaches, further comprising mounting the adhesive-coated tape to a backside of the semiconductor wafer and singulating the semiconductor wafer from an active surface thereof (figures 1 and 2; col. 2, lines 48-50; col. 3, lines 1-33).

Pertaining to claim 11, Akram teaches, wherein mounting the adhesive-coated tape comprises mounting a tape bearing a UV-sensitive adhesive thereon (figure 1; col. 2, lines 48-50).

Pertaining to claim 12, Akram teaches, further comprising exposing the UV-sensitive adhesive prior to removing the at least some individual components, but for a portion on the

adhesive-coated tape extending over the ring of material (figure 8; col. 3, lines 1-33; col. 4, lines 50-67; col. 5, lines 1-4).

Pertaining to claim 13, Akram teaches, wherein the semiconductor wafer is singulated using one of laser cutting, water cutting and sawing (col. 3, lines 1-12).

Pertaining to claim 14, Akram teaches, further comprising discarding the ring of material, any remaining individual components and the adhesive-coated tape after removing the at least some individual components (col. 4, lines 17-26).

Pertaining to claim 29, Akram teaches, a method of processing a semiconductor wafer, comprising: singulating a semiconductor wafer **16** into individual components **20** while leaving an uncut peripheral ring of material thereabout (figure 1; col. 2, lines 60-67; col. 3, lines 1-12.

Pertaining to claim 30, Akram teaches, further including removing at least some singulated individual components therefrom (figure 8; col. 4, lines 50-67; col. 5, lines 1-4).

Pertaining to claim 31, Akram teaches, further including gripping the uncut peripheral ring of material while removing the at least some singulated individual components therefrom (col. 4, lines 17-67; col. 5, lines 1-4).

Pertaining to claim 32, Akram teaches, further comprising defining the uncut peripheral ring of material from semiconductor material (figure 1; col. 2, lines 50-67).

Pertaining to claim 33, Akram teaches, further comprising defining the uncut peripheral ring of material at least in part from a polymer disposed about the semiconductor wafer (figures 1 and 2; col. 2, lines 48-67; col. 3, lines 1-33).

Pertaining to claim 34, Akram teaches, further comprising defining the uncut peripheral ring of material in part from semiconductor material and in part from a polymer disposed about a periphery of the semiconductor wafer (figures 1 and 2; col. 2, lines 48-67; col. 3, lines 1-12).

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

Claim 25 is rejected under 35 U.S.C. 102(e) as being anticipated by Tandy et al., US Patent 6,524,881.

Tandy discloses the semiconductor method as claimed. See figures 1A-6, and corresponding text, where Tandy teaches, pertaining to claim 25, a method for processing a semiconductor wafer, comprising: singulating a semiconductor wafer **10** into individual components **20** and removing at least some singulated individual components without using a film frame (figures 1A-1B and 4A-6; col. 5, lines 12-29; col. 6, lines 44-67; col. 8, lines 24-65).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 7-9 and 35-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akram US Patent 6,140,151 in view of Oka US Patent 6,551,904.

Akram discloses the semiconductor method substantially as claimed. See preceding rejection of claims 1-6, 10-14 and 29-34 under 35 U.S.C. 102(b). In addition, Akram shows, pertaining to claim 8, further comprising mounting the adhesive-coated tape to an active surface of the semiconductor wafer and singulating the semiconductor wafer from a backside thereof after backgrinding (figure 1; col. 2, lines 48-50; figures 1 and 2; col. 3, lines 1-33). Also, Akram shows, pertaining to claim 9, further comprising mounting the adhesive-coated tape to a backside of the semiconductor wafer and singulating the semiconductor wafer from an active surface thereof (figures 1 and 2; col. 2, lines 48-50; col. 3, lines 1-33).

However, Akram fails to show, pertaining to claim 7, further comprising backgrinding the semiconductor wafer prior to singulation. In addition, Akram fails to show pertaining to claim 35, wherein the semiconductor wafer is a 300 mm semiconductor wafer and further including handling the 300 mm semiconductor wafer using equipment sized to handle a 200 mm semiconductor wafer saw chuck. Also, Akram fails to show, pertaining to claim 36, further including singulating the 300 mm semiconductor wafer using a 200 mm semiconductor wafer

saw chuck. Akram fails to show, pertaining to claim 37, further including holding the 300 mm semiconductor wafer in a 200 mm semiconductor wafer pick-and-place machine chuck while removing the at least some singulated individual components therefrom. In addition, Akram fails to show, pertaining to claim 38, a method of using a 300 mm semiconductor wafer, including handling the 300 mm semiconductor wafer with equipment sized to handle 200 mm semiconductor wafers. Finally, Akram fails to show, pertaining to claim 39, further including processing the 300 mm semiconductor wafer with equipment sized to handle 200 mm semiconductor wafers.

Oka teaches, in figures 1A-7H, and corresponding text, a similar method where conventionally the semiconductor wafers are grinded to a desired thickness of 300 mm prior to singulation (col. 1, lines 19-66; col. 2, lines 9-15).

It would have been obvious to one of ordinary skill in the art to incorporate the following steps: further comprising backgrinding the semiconductor wafer prior to singulation; wherein the semiconductor wafer is a 300 mm semiconductor wafer and further including handling the 300 mm semiconductor wafer using equipment sized to handle a 200 mm semiconductor wafer saw chuck; further including singulating the 300 mm semiconductor wafer using a 200 mm semiconductor wafer saw chuck; further including holding the 300 mm semiconductor wafer in a 200 mm semiconductor wafer pick-and-place machine chuck while removing the at least some singulated individual components therefrom; a method of using a 300 mm semiconductor wafer, including handling the 300 mm semiconductor wafer with equipment sized to handle 200 mm semiconductor wafers; further including processing the 300 mm semiconductor wafer with equipment sized to handle 200 mm semiconductor wafers, in the method of Akram, pertaining to

claims 7 and 35-39, according to the teachings of Oka, with the motivation of conventionally preparing the semiconductor wafer for further packaging processing techniques such as chip formation. In addition, since the semiconductor wafer size is 300 mm the advantage would be greater production in the number of chips produced, resulting in an improvement of throughput chip manufacturing. Finally, since Oka teaches, that the semiconductor wafers are conventionally formed at a size of 300 mm, having equipment to accommodate handling a wafer of this size is obviously well known in the art of semiconductor manufacturing.

Claims 26-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tandy et al., US Patent 6,524,881 in view of Oka US Patent 6,551,906.

Tandy discloses the semiconductor method substantially as claimed. See preceding rejection of claim 25 under 35 U.S.C. 102(e).

However, Tandy fails to show, pertaining to claim 26, wherein the semiconductor wafer is a 300 mm semiconductor wafer and further including handling the 300 mm semiconductor wafer using equipment sized to handle 200 mm semiconductor wafers. In addition, Tandy fails to show, pertaining to claim 27 further including singulating the 300 mm semiconductor wafer using a 200 mm semiconductor wafer saw chuck. Finally, Tandy fails to show, pertaining to claim 28, further including holding the 300 mm semiconductor wafer in a 200 mm semiconductor wafer pick-and-place machine chuck while removing the at least some singluated individual components therefrom.

Oka teaches, in figures 1A-7H, and corresponding text, a similar method where conventionally the semiconductor wafers are grinded to a desired thickness of 300 mm prior to singulation (col. 1, lines 19-66; col. 2, lines 9-15).

It would have been obvious to one of ordinary skill in the art to incorporate the following steps: wherein the semiconductor wafer is a 300 mm semiconductor wafer and further including handling the 300 mm semiconductor wafer using equipment sized to handle 200 mm semiconductor wafers; further including singulating the 300 mm semiconductor wafer using a 200 mm semiconductor wafer saw chuck; further including holding the 300 mm semiconductor wafer in a 200 mm semiconductor wafer pick-and-place machine chuck while removing the at least some singulated individual components therefrom, in the method of Akram, pertaining to claims 26-28, according to the teachings of Oka, with the motivation of conventionally preparing the semiconductor wafer for further packaging processing techniques such as chip formation. In addition, since the semiconductor wafer size is 300 mm the advantage would be greater production in the number of chips produced, resulting in an improvement of throughput chip manufacturing. Finally, since Oka teaches, that the semiconductor wafers are conventionally formed at a size of 300 mm, having equipment to accommodate handling a wafer of this size is obviously well known in the art of semiconductor manufacturing.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stanetta Isaac
Patent Examiner
May 24, 2005

MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER